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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,964	FUJIMOTO ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21,23-25,27,29-39 and 44-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21,23-25,27,29-39 and 44-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed December 30, 2008 in response to the Office action dated September 30, 2008. Claims 21, 36-39, 44-53 have been amended. Claims 21, 23-25, 27, 29-39, and 44-54 are pending in this application.

OBJECTIONS

Claims

1. In view of Applicant's amendments, the objections to **claims 38 and 39** have been withdrawn.

REJECTIONS NOT BASED ON PRIOR ART

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. **Claims 21, 23-25, 27, 29-39, and 44-54** are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 21-25, 33, 35, 37-42, 57, and 58 of copending Application No. 11/031,556. Although the conflicting claims are not identical, they are not patentably distinct from each other because both applications recite non-patentably distinct storage systems comprising disk drives/units, interface adapters/units, processor adapters/units, cache memory adapter/unit, switch adapter/unit, and microprocessors.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21-28 and 30-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis et al. (U.S. Patent 6,343,324) (hereinafter "Hubis") in view of Klein (U.S. Patent 6,108,732) and Yamamoto et al. (U.S. Patent Application Publication 2001/0023463) (hereinafter "Yamamoto").

6. **As per claim 21**, Hubis discloses a storage system comprising:

a plurality of disk drives configuring at least one logical volume (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter including at least one processor and controlling to store data, which are sent from at least one host computer to said logical volume (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180); *It should be noted that the "Processor 180" is analogous to the "processor adapter."*

a plurality of first interface adapters each coupled to said at least one host computer and receiving a write request and data sent from said at least one host computer and sending a first control information related to said write request to at least one of said processor adapters and sending data received at each of said first interface adapters based on a second control information sent from said at least one processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1 – 184-M); *It should be noted that the "I/O Processors 184-1-M" are analogous to the "plurality of first interface adapters."*

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186); *It should be noted that the "Data Cache Memory" is analogous to the "cache memory adapter."*

a plurality of second interface adapters each receiving data stored in said cache memory adapter from said cache memory adapter based on a third control information sent from said at least one processor adapter and storing data received at each of said

second interface adapters in said disk drives (col. 16, lines 3-6; Fig. 2A, element 185-1); *It should be noted that the "I/O Processors 185-1-M" are analogous to the "plurality of second interface adapters."*

a switch adapter coupled to said processor adapters, said first interface adapters, said cache memory adapter and said second interface adapters and relaying data between said first interface adapters and said cache memory adapter and relaying data between said cache memory adapter and said second interface adapters (col. 15, lines 63-66; Fig. 2A, element 183); *It should be noted that the "PCI Bus Interface and Memory Controller" is analogous to the "switch adapter."*

wherein said switch adapter relays said first and said second control information between said processor adapters and said first interface adapters and relays said third control information between said processor adapters and said second interface adapters (col. 15, lines 63-66; col. 16, lines 6-9); *It should be noted that the Processor is coupled to the system only through the PCI Bus Interface and Memory Controller, therefore, all control information is required to be relayed via the PCI Bus Interface and Memory Controller.*

Hubis does not disclose a plurality of processor adapters;

wherein the number of said processor adapters are increased or decreased independently of the first and second interface adaptor, the memory adaptor and the switch adaptor, based on a required performance.

Klein discloses a plurality of processor adapters (col. 3, lines 23-29; Fig. 1, elements 102, 108, 114, and 120); *It should be noted that the "CPUs" are analogous to the "processor adapters."*

wherein the number of said processor adapters are increased or decreased independently of the first and second interface adaptor, the memory adaptor and the switch adaptor, based on a required performance (col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4).

Hubis and Klein are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Klein's adding or removing processor modules technique to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of both allowing a CPU to be removed without shutting the computer system down as well as allowing a CPU to be inserted and initialized while the computer system is operating.

The combination of Hubis/Klein does not disclose each of said processor adapters has a plurality of microprocessors and, each of said microprocessors is assigned to operate either a first processing load sent from said first interface adapters or a second processing load sent from said second interface adapters in accordance

with an amount of the first processing load and an amount of the second processing load.

Yamamoto discloses a processor adapter has a plurality of microprocessors and, each of said microprocessors is assigned to operate either a first processing load sent from a host computer or a second processing load sent from said second interface adapters in accordance with an amount of the first processing load and an amount of the second processing load (paragraphs 0020 and 0033; Figs. 5-8). *It should be noted that the "controller" is analogous to the "processor adapter."*

The combination of Hubis/Klein and Yamamoto are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Yamamoto's microprocessors within Hubis/Klein's processor adapters such that each of said microprocessors is assigned to operate a first processing load sent from said first interface adapters in accordance with an amount of the first processing load. The motivation for doing so would have been to provide multiple, parallel data paths between multiple processors and physical storage which in turn, provides almost instantaneous access to data.

7. **As per claim 23**, the combination of Hubis/Klein/Yamamoto discloses said processor adapters are assigned to a process of at least one of said first interface adapters and a process of at least one of said second interface adapters (Hubis, col. 16, lines 6-9).

8. **As per claim 24**, the combination of Hubis/Klein/Yamamoto discloses said at least one processor adapter is assigned to said plurality of first interface adapters (Hubis, col. 16, lines 6-9).

9. **As per claim 25**, the combination of Hubis/Klein/Yamamoto discloses said at least one processor adapter is assigned to said plurality of second interface adapters (Hubis, col. 16, lines 6-9).

10. **As per claim 27**, the combination of Hubis/Klein/Yamamoto discloses it is possible to change the number of said processor adapters on storing data in said disk drives (Klein, col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4).

11. **As per claim 30**, the combination of Hubis/Klein/Yamamoto discloses said first control information is used to notify said at least one processor adapter of receiving said write request (Hubis, col. 15, lines 10-25).

12. **As per claim 31**, the combination of Hubis/Klein/Yamamoto discloses said at least one processor adapter detects an area of said memory in which data of said logical volume need to be stored in accordance with said received first control information (Hubis, col. 15, lines 19-25; col. 16, line 67 – col. 17, line 9). *It should be noted that it is inherently required Processor 180 detect/recognize an area of the Data Cache Memory in order to allocate space for storing data in the Cache Memory during a write task.*

13. **As per claim 32**, the combination of Hubis/Klein/Yamamoto discloses said second control information includes information related to an area of said memory in

which data received at said first interface adapter need to be stored (Hubis, col. 15, lines 19-25; col. 16, line 67 – col. 17, line 9). I*t should be noted that it is inherently required Processor 180 allocate/reserve an area of the Data Cache Memory in order to store data in the Cache Memory during a write task.*

14. **As per claim 33**, the combination of Hubis/Klein/Yamamoto discloses said at least one processor adapter finds an area of said disk drives related to said logical volume for storing data of said logical volume based on said received first control information (Hubis, col. 15, lines 23-25; col. 16, lines 6-9).

15. **As per claim 34**, the combination of Hubis/Klein/Yamamoto discloses said third control information includes information related to an area of said disk drives in which data received at said second interface adapter need to be stored (Hubis, col. 15, lines 23-25; col. 16, lines 6-9).

16. **As per claim 35**, the combination of Hubis/Klein/Yamamoto discloses said at least one processor adapter controls to create a parity data of RAID (Redundant Array of Inexpensive Disks) from data received at least one of said first interface adapters (Hubis, col. 4, line 64 – col. 5, line 3).

17. **As per claim 36**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive configuring at least one logical volume (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter each including at least one processor and controlling to store data by determining a location at which the data should be stored, the data being

sent from said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving a write request and data sent from said host computer and sending a first control information related to said write request to said processor adapter and sending data received at said first interface adapter based on a second control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1); *It should be noted that the "I/O Processor 184-1" is analogous to the "first interface adapter."*

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter receiving data stored in said cache memory adapter from said cache memory adapter based on a third control information sent from said processor adapter and storing data received at said second interface adapter in said disk drive (col. 16, lines 3-6; Fig. 2A, element 185-1); *It should be noted that the "I/O Processor 185-1" is analogous to the "second interface adapter."*

a switch adapter coupled to said processor adapter, said first interface adapter, said cache memory adapter and said second interface adapter and relaying said data among said first interface adapter, said cache memory adapter and said second interface adapter (col. 15, lines 63-66; Fig. 2A, element 183);

wherein said switch adapter relays said first and said second control information between said processor adapter and said first interface adapter and relays said third control information between said processor adapter and said second interface adapter (col. 15, lines 63-66; col. 16, lines 6-9); *It should be noted that the Processor is coupled to the system only through the PCI Bus Interface and Memory Controller, therefore, all control information is required to be relayed via the PCI Bus Interface and Memory Controller.*

Hubis does not disclose a plurality of processor adapters;

wherein the number of said processor adaptors are increased or decreased based on a required performance, even though the number of said first interface adapter, said cache memory adapter and said second interface adapter are not increased or decreased.

Klein discloses a plurality of processor adapters (col. 3, lines 23-29; Fig. 1, elements 102, 108, 114, and 120);

wherein the number of said processor adaptors are increased or decreased based on a required performance, even though the number of said first interface adapter, said cache memory adapter and said second interface adapter are not increased or decreased (col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4).

Hubis and Klein are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Klein's adding or removing processor modules technique to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of both allowing a CPU to be removed without shutting the computer system down as well as allowing a CPU to be inserted and initialized while the computer system is operating.

The combination of Hubis/Klein does not disclose each of said processor adapters has a plurality of microprocessors and, each of said microprocessors is assigned to operate either a first processing load sent from said first interface adapters or a second processing load sent from said second interface adapters in accordance with an amount of the first processing load and an amount of the second processing load.

Yamamoto discloses a processor adapter has a plurality of microprocessors and, each of said microprocessors is assigned to operate either a first processing load sent from a host computer or a second processing load sent from said second interface adapters in accordance with an amount of the first processing load and an amount of the second processing load (paragraphs 0020 and 0033; Figs. 5-8).

The combination of Hubis/Klein and Yamamoto are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Yamamoto's microprocessors within Hubis/Klein's processor adapters such that each of said microprocessors is assigned to operate a first processing load sent from said first interface adapters in accordance with an amount of the first processing load. The motivation for doing so would have been to provide multiple, parallel data paths between multiple processors and physical storage which in turn, provides almost instantaneous access to data.

18. **As per claim 37**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive configuring at least one logical volume (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter including at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving data sent from said host computer and sending data received at said first interface adapter based on a first control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter receiving data stored in said cache memory adapter from said cache memory adapter based on a second control information sent from said processor adapter and storing data received at said second interface adapter in said disk drive (col. 16, lines 3-6; Fig. 2A, element 185-1);

a switch adapter coupled to said processor adapter, said first interface adapter, said cache memory adapter and said second interface adapter and relaying data of said logical volume among said first interface adapter, said cache memory adapter and said second interface adapter and not relaying data of said logical volume to said processor adapter (col. 15, lines 63-66; Fig. 2A, element 183); *It should be noted that when the host sends a read request to the logical volumes, Processor 180 does not receive the read data itself, but rather controls the process of sending the read data back to the host.*

wherein said switch adapter relays said first control information between said processor adapter and said first interface adapter and relays said second control information between said processor adapter and said second interface adapter (col. 15, lines 63-66; col. 16, lines 6-9); *It should be noted that the Processor is coupled to the system only through the PCI Bus Interface and Memory Controller, therefore, all control information is required to be relayed via the PCI Bus Interface and Memory Controller.*

Hubis does not disclose a plurality of processor adapters;

wherein it is possible to change the number of said processor adapters, independently of the first and second interface adaptors, the memory adaptor and the

switch adaptor, upon storing on storing data in said disk drive and based on a required performance.

Klein discloses a plurality of processor adapters (col. 3, lines 23-29; Fig. 1, elements 102, 108, 114, and 120);

wherein it is possible to change the number of said processor adapters, independently of the first and second interface adaptors, the memory adaptor and the switch adaptor, upon storing on storing data in said disk drive and based on a required performance (col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4).

Hubis and Klein are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Klein's adding or removing processor modules technique to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of both allowing a CPU to be removed without shutting the computer system down as well as allowing a CPU to be inserted and initialized while the computer system is operating.

The combination of Hubis/Klein does not disclose each of said processor adapters has a plurality of microprocessors and, each of said microprocessors is assigned to operate either a first processing load sent from said first interface adapters

or a second processing load sent from said second interface adapters in accordance with an amount of the first processing load and an amount of the second processing load.

Yamamoto discloses a processor adapter has a plurality of microprocessors and, each of said microprocessors is assigned to operate either a first processing load sent from a host computer or a second processing load sent from said second interface adapters in accordance with an amount of the first processing load and an amount of the second processing load (paragraphs 0020 and 0033; Figs. 5-8).

The combination of Hubis/Klein and Yamamoto are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Yamamoto's microprocessors within Hubis/Klein's processor adapters such that each of said microprocessors is assigned to operate a first processing load sent from said first interface adapters in accordance with an amount of the first processing load. The motivation for doing so would have been to provide multiple, parallel data paths between multiple processors and physical storage which in turn, provides almost instantaneous access to data.

19. **As per claim 38**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive configuring at least one logical volume (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter including at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter coupled to said first interface adapter, said processor adapter, and said cache memory adapter (col. 16, lines 3-6; Fig. 2A, element 185-1);

a switch adapter coupled to said processor adapter, said first interface adapter, said cache memory adapter and said second interface adapter (col. 15, lines 63-66; Fig. 2A, element 183);

wherein said switch adapter relays data between said first interface adapter and said second interface adapter via said cache memory adapter among said first interface adapter, said processor adapter, said cache memory adapter and said second interface adapter based on control information transferred among said first interface adapter, said processor adapter and said second interface adapter of said first interface adapter, said processor adapter, said cache memory adapter, and said second interface adapter (col. 15, lines 63-66; col. 15, line 67 – col. 16, line; Fig. 2A, elements 183 and 186). *It should*

be noted that Data Cache Memory buffers any data sent between I/O Processor 184-1 and I/O Processor 185-1.

Hubis does not disclose a plurality of processor adapters;

wherein the number of said processor adapters are increased or decreased independently of the first and second interface adaptor, the memory adaptor and the switch adaptor, based on a required performance.

Klein discloses a plurality of processor adapters (col. 3, lines 23-29; Fig. 1, elements 102, 108, 114, and 120); *It should be noted that the "CPUs" are analogous to the "processor adapters."*

wherein the number of said processor adapters are increased or decreased independently of the first and second interface adaptor, the memory adaptor and the switch adaptor, based on a required performance (col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4).

Hubis and Klein are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Klein's adding or removing processor modules technique to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of both allowing a CPU to be removed without shutting the

computer system down as well as allowing a CPU to be inserted and initialized while the computer system is operating.

The combination of Hubis/Klein does not disclose each of said processor adapters has a plurality of microprocessors and, each of said microprocessors is assigned to operate either a first processing load sent from said first interface adapters or a second processing load sent from said second interface adapters in accordance with an amount of the first processing load and an amount of the second processing load.

Yamamoto discloses a processor adapter has a plurality of microprocessors and, each of said microprocessors is assigned to operate either a first processing load sent from a host computer or a second processing load sent from said second interface adapters in accordance with an amount of the first processing load and an amount of the second processing load (paragraphs 0020 and 0033; Figs. 5-8).

The combination of Hubis/Klein and Yamamoto are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Yamamoto's microprocessors within Hubis/Klein's processor adapters such that each of said microprocessors is assigned to operate a first processing load sent from said first interface adapters in accordance with an amount of the first processing load. The motivation for doing so would have been to provide multiple, parallel data paths between multiple processors and physical storage which in turn, provides almost instantaneous access to data.

20. **As per claim 39**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive configuring at least one logical volume (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter including at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving a write request and data sent from said host computer and sending a first control information related to said write request to said processor adapter and sending data received at said first interface adapter based on a second control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter receiving data stored in said cache memory adapter from said cache memory adapter based on a third control information sent from said processor adapter and storing data received at said second interface adapter in said disk drive (col. 16, lines 3-6; Fig. 2A, element 185-1);

wherein said processor adapter coupled to said first interface adapter and said second interface adapter and sends said second control information to said first interface adapter and sends said third control information to said second interface adapter (col. 16, lines 6-9);

wherein said first interface adapter sends data to said cache memory adapter among said processor adapter, said cache memory adapter and said second interface adapter (col. 15, line 67 – col. 16, line 3);

wherein said second interface adapter receives data from said cache memory adapter among said processor adapter, said cache memory adapter and said first interface adapter (col. 16, lines 3-6);

wherein said cache memory adapter receives data from said first interface adapter and said second interface adapter among said processor adapter, said first interface adapter and said second interface adapter (col. 15, line 67 – col. 16, line 6);

Hubis does not disclose a plurality of processor adapters;

wherein the number of said processor adapters are increased or decreased independently of the first and second interface adaptor and the memory adaptor, based on a required performance.

Klein discloses a plurality of processor adapters (col. 3, lines 23-29; Fig. 1, elements 102, 108, 114, and 120); *It should be noted that the "CPUs" are analogous to the "processor adapters."*

wherein the number of said processor adapters are increased or decreased independently of the first and second interface adaptor and the memory adaptor, based

on a required performance (col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4).

Hubis and Klein are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Klein's adding or removing processor modules technique to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of both allowing a CPU to be removed without shutting the computer system down as well as allowing a CPU to be inserted and initialized while the computer system is operating.

The combination of Hubis/Klein does not disclose each of said processor adapters has a plurality of microprocessors and, each of said microprocessors is assigned to operate either a first processing load sent from said first interface adapters or a second processing load sent from said second interface adapters in accordance with an amount of the first processing load and an amount of the second processing load.

Yamamoto discloses a processor adapter has a plurality of microprocessors and, each of said microprocessors is assigned to operate either a first processing load sent from a host computer or a second processing load sent from said second interface

adapters in accordance with an amount of the first processing load and an amount of the second processing load (paragraphs 0020 and 0033; Figs. 5-8).

The combination of Hubis/Klein and Yamamoto are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Yamamoto's microprocessors within Hubis/Klein's processor adapters such that each of said microprocessors is assigned to operate a first processing load sent from said first interface adapters in accordance with an amount of the first processing load. The motivation for doing so would have been to provide multiple, parallel data paths between multiple processors and physical storage which in turn, provides almost instantaneous access to data.

21. **As per claims 44-52**, the combination of Hubis/Klein/Yamamoto discloses the cache memory adapter includes a control information memory module in which information for controlling data transfer is stored (Hubis, col. 15, line 67 – col. 16, line 3; col. 8, lines 2-5; Fig. 2A, element 186).

22. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis in view of Klein and Yamamoto as applied to claim 21 above, and further in view of Kuchta et al. (U.S. Patent 6,014,319) (hereinafter "Kuchta").

23. **As per claim 29**, the combination of Hubis/Klein does not disclose a first portion of said processor adapters are assigned to a process of at least one of said first interface adapters;

a second portion of said processor adapters are assigned to a process of at least one of said second interface adapters;

a proportion between said first portion and said second portion is decided in accordance with a proportion between a performance of said at least one first interface adapter and a performance of said at least one second interface adapter.

Kutcha discloses a first portion of said processor adapters are assigned to a process of at least one of said first interface adapters (col. 7, lines 15-18; Fig. 2A, element 245; Fig. 2B, elements 211-212); *It should be noted that "I/O modules 211-212" are analogous to the "first portion of processor adapters" and "I/O cards 245" are analogous to "first interface adapters."*

a second portion of said processor adapters are assigned to a process of at least one of said second interface adapters (col. 7, lines 35-38; Fig. 2A, element 246; Fig. 2B, elements 209-210); *It should be noted that "I/O modules 209-210" are analogous to the "second portion of processor adapters" and "I/O cards 246" are analogous to "second interface adapters."*

a proportion between said first portion and said second portion is decided in accordance with a proportion between a performance of said at least one first interface adapter and a performance of said at least one second interface adapter (col. 5, lines 59-63). *It should be noted that amount of I/O modules 209-210 versus the amount of I/O modules 211-212 (i.e. a proportion between said first portion and said second portion) is based on performance characteristics.*

The combination of Hubis/Klein and Kuchta are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Kuchta's additional I/O modules within Hubis/Klein's storage system. The motivation for doing so would have been to provide later system enhancements (Kuchta, col. 5, lines 49-50).

24. Claims 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis in view of Klein, Yamamoto, and Matsunami et al. (U.S. Patent Application Publication 2002/0091898) (hereinafter "Matsunami").

25. **As per claim 53**, Hubis discloses a storage system comprising:

a plurality of disk drives (col. 7, lines 27-28; Fig. 2, element 108);

a plurality of first interface units each coupled to said at least one host computer and receiving a write request and data sent from said at least one host computer (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1 – 184-M);

a plurality of second interface units each coupled to said plurality of disk drives (col. 16, lines 3-6; Fig. 2A, element 185-1);

a processor unit separated from said first interface units and said second interface units and each having at least one processor (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a memory unit having at least one memory, said memory temporarily storing data sent from said first interface units (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a switch unit coupled to said first interface units, said second interface units, and said processor unit (col. 15, lines 63-66; Fig. 2A, element 183).

Hubis does not disclose a storage system comprising a first cluster system and a second cluster system,

a plurality of processor units;

wherein the switch unit of the first cluster system is coupled to the switch of the second cluster system by a communication path;

wherein the number of said processor units of the first cluster system and said second cluster system can be increased or decreased, independently of the first and second interface units, the memory units and the switch unit, based on a required performance.

Klein discloses a plurality of processor units (col. 3, lines 23-29; Fig. 1, elements 102, 108, 114, and 120);

wherein the number of said processor units of the first cluster system and said second cluster system can be increased or decreased, independently of the first and second interface units, the memory units and the switch unit, based on a required performance (col. 4, line 56 – col. 5, line 37; col. 5, line 49 – col. 6, line 12; Figs. 3 and 4).

Hubis and Klein are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Klein's adding or removing processor modules technique to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of both allowing a CPU to be removed without shutting the computer system down as well as allowing a CPU to be inserted and initialized while the computer system is operating.

The combination of Hubis/Klein does not disclose a storage system comprising a first cluster system and a second cluster system,

wherein the switch unit of the first cluster system is coupled to the switch of the second cluster system by a communication path.

Matsunami discloses a storage system comprising a first cluster system and a second cluster system (paragraph 0043; paragraph 0070; Fig. 14, elements 10 and 20); *It should be noted that each "disk array switch" combined with its respective "disk array subset" comprises a "cluster."*

wherein the switch unit of the first cluster system is coupled to the switch of the second cluster system by a communication path (paragraph 0043; paragraph 0070; Fig. 3, elements 201 and 2040; Fig. 14, element 2040). *It should be noted that the "crossbar*

switch" is analogous to the "switch unit" and the "Intercluster I/F" is analogous to the "communication path."

The combination of Hubis/Klein and Matsunami are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Matsunami's clustered storage system and Hubis/Klein's array controller and processor modules such that the storage system comprises a first cluster and a second cluster, each cluster comprising an array controller, a plurality of processor modules, and a plurality of disk drives, because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing a disk storage system that responds easily to needs for high reliability and future expansion.

The combination of Hubis/Klein/Matsunami does not disclose each of said processor adapters has a plurality of microprocessors and, each of said microprocessors is assigned to operate either a first processing load sent from said first interface adapters or a second processing load sent from said second interface adapters in accordance with an amount of the first processing load and an amount of the second processing load.

Yamamoto discloses a processor adapter has a plurality of microprocessors and, each of said microprocessors is assigned to operate either a first processing load sent from a host computer or a second processing load sent from said second interface

adapters in accordance with an amount of the first processing load and an amount of the second processing load (paragraphs 0020 and 0033; Figs. 5-8).

The combination of Hubis/Klein/Matsunami and Yamamoto are analogous art because they are from the same field of endeavor, that being computer storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Yamamoto's microprocessors within Hubis/Klein/Matsunami's processor adapters such that each of said microprocessors is assigned to operate a first processing load sent from said first interface adapters in accordance with an amount of the first processing load. The motivation for doing so would have been to provide multiple, parallel data paths between multiple processors and physical storage which in turn, provides almost instantaneous access to data.

26. **As per claim 54**, the combination of Hubis/Klein/Matsunami/Yamamoto discloses said processor units in said first cluster system can instruct said plurality of first interface units and the plurality of second interface units of said second cluster system to transfer a data (Matsunami, paragraph 0070).

Response to Arguments

27. Applicant's arguments filed December 30, 2008 with respect to **claims 21, 23-25, 27, 29-39, and 44-54** have been considered but are moot in view of the new grounds of rejection above.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 21, 23-25, 27, 29-39, and 44-54** have received an action on the merits and are subject of a final action.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
April 2, 2009

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185